Docket No.: 21806-00070-US1
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Eric Adler et al.

Application No.: 10/697,012 Confirmation No.: 8254

Filed: October 31, 2003 Art Unit: 2812

For: SEMICONDUCTOR DEVICE AND METHOD FOR MAKING THE DEVICE HAVING AN ELECTRICALLY MODULATED CONDUCTION CHANNEL

Examiner: R. E. Pompey

REPLY BRIEF

MS Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

This Reply Brief is filed in response to the Examiner's Answer mailed June 1, 2006. Appellant has chosen to limit this reply the errors in the rejection of claim 20 and claim 26. More specifically the errors in the attribution of certain subject matter to the cited references of U.S. Patent No. 5,241,210 (Nakagawa et al.), U.S. Patent No. 6,118,152 (Yamaguchi et al.) and U.S. Patent No. 3,813,586 (Conner) involved in the rejections of claims 20-27. However, the rejections not specifically mentioned herein are also subject to the same infirmities. Appellant respectfully submits the Examiner's Answer has: (1) ignored subject matter specifically defined in the claims; (2) has alleged subject matter is disclosed in the references when it is not disclosed therein.

INTRODUCTION

The present invention is a semiconductor device having an electrically modulated conduction channel. The semiconductor device is located within a trench structure formed in a substrate of a metal-oxide semiconductor (MOS) integrated circuit. The semiconductor device may be a Field Effect Transistor (FET), having a gate deposited over a diffusion region is located within the trench structure. The diffusion region is electrically modulated by applying a control voltage to terminals connected to the trench structure and the substrate. In this way, the channel width below the gate can be modulated by the application of the control voltage, producing a change in the resistance of the channel and the transistor gain. That is, the gain of the semiconductor device may effectively be set by varying the control voltage applied to the terminals of the trench structure and the substrate.

In the specification and figures of U.S. Patent Application Publication US 2004/0092109A1, a transistor implementation of the present invention having an electrically modulated channel is shown in FIG. 1A through FIG. 1D. In particular, FIG. 1A and FIG. 1B show a diffusion region **11** formed in an integrated circuit substrate **25** and surrounded by a trench **12**. Further, independent claim 20 may be annotated in accordance with the reference numbers of the specification and figures to describe the invention as follows:

> [a] method for making a semiconductor chip comprising:
> forming a diffusion region **11** in a semiconductor substrate **25**;
> forming an insulated trench structure **12** in said substrate **25** which surrounds said diffusion region **11**; and
> forming electrical connections **21, 25** on said trench structure **12** and said substrate **25** which receive a control voltage whereby an electric field is produced to control a current flowing in said diffusion region **11**.

Alternatively, the trench structure may include multiple diffusion regions, each of which serve as a resistor controlled from a common control voltage applied to a gate electrode. FIG. 6A shows in greater detail the construction of a given trench **56** and the individual resistors (i.e., references **50-54** of FIG. 5) within the trench **56**. Referring now to

FIG. 6A, the resistors **50-54** each comprise a diffusion layer **59**, shown as doped N+ layer, formed within a well of polysilicon **60** deposited within the trench **56**. The diffusion layer **59** is connected to contacts **61** and **64**, formed through an oxide layer **60**. Contacts **61** and **64** provide for connections to the resistor. The trench **56** is filled with polysilicon **57**, and each of the resistors **50-54** are separated from the trench **56** by a thin oxide layer **56**. Accordingly, a potential applied between terminal **63** in contact with the trench **56** and the substrate **72** provides an electrostatic field for modulating the width of each the resistors **50-54** in a bank. Further, claim 26 can be annotated in accordance with the reference numbers and description to describe the present invention as follows:

> [a] method for making a semiconductor chip comprising:
> forming multiple diffusion regions **59** that are surrounded by multiple trench structures **56** on a substrate **72**; and
> forming multiple contacts **61, 64** on each of said trench structures **56** and said substrate for controlling current through said diffusion regions **59**.

As noted above, the Appellant respectfully submits the Examiner's Answer has: (1) ignored subject matter specifically defined in the claims; and (2) has alleged subject matter is disclosed in the references that cannot be found therein.

(1) THE REJECTIONS OF CLAIMS 20-27 ARE FLAWED IN THAT THEY IGNORE SIGNIFICANT CLAIMED SUBJECT MATTER AND ATTRIBUTES TO THE NAKAGAWA et al. REFERENCE SUBJECT MATTER WHICH CANNOT BE FOUND THEREIN

Claim 20 was rejected under 35 USC 102 as anticipated by Nakagawa et al. Page 3, paragraph 2 of the Examiner's Answer discusses this rejection. Section 1208 of the MPEP requires that for each rejection under 35 USC 102, the Examiner's Answer shall explain why the rejected claims are anticipated "pointing out where *all of the specific limitations* recited in the rejected claims are found in *the prior art* relied upon in the rejection." (emphasis added). However, the rejection of claim 20 in the Examiner's Answer fails to comply with this requirement.

The Examiner's Answer states generally at page 3, paragraph 2, that Nakagawa et al. discloses a diffusion region (**59a, fig. 17**). More specifically at page 5, the Examiner's Answer states that Nakagawa et al. discloses: a trench structure (**53, fig. 17**) with an electrode formed on it and a substrate (**54a, fig. 17**) with an electrode (**63a, fig. 17**), wherein a control voltage is applied, which will create an electric field.

The Examiner's Answer states generally at page 4, paragraph 3, that Yamaguchi discloses a diffusion region (**13a, fig. 1**). More specifically at page 6, the Examiner's Answer states that Yamaguchi discloses: a trench structure (**5, fig. 1**) with an electrode formed on the trench structure (**19a, 19b, fig. 1**) and a substrate with an electrode (**18, fig. 1**), wherein a control voltage is applied, which will create an electric field.

However, neither Nakagawa et al. nor Yamaguchi discloses the above discussed electrodes as "receiving a control voltage" or that "an electric field is produced," in the above discussed diffusion region, as explicitly recited in claim 20 and in similar language in claim 26. In addition, it is respectfully submitted that even if a control voltage is applied to the above-discussed electrodes, as disclosed by Nakagawa et al. and Yamaguchi, it would *not* create an electric field in diffusion region (**59a, fig. 17**) due to differences in the structure and operation of Nakagawa et al. and Yamaguchi, as compared to the claimed invention. In particular, the electrodes formed on the trench structure of Nakagawa et al. are also tied to a third electrode (**62a, fig. 17**) and the trench electrodes (**19a, 19b, fig. 1**) of Yamaguchi are tied to ground.

In contrast to Nakagawa et al. and Yamaguchi the present invention claims, as recited in claim 20:

> forming electrical connections on said trench structure *and* said substrate which *receive a control voltage whereby an electric field is produced to control a current flowing in said diffusion region* (emphasis added);

and as recited in claim 26:

> forming multiple contacts on each of said trench structures *and* said substrate *for controlling current through said diffusion regions* (emphasis added).

That is, Applicants respectfully submit that neither Nakagawa et al. nor Yamaguchi discloses a device with *both* a "trench structure" with a trench terminal connection **21** *and* "substrate" with substrate terminal connection **22**, as in the present invention; wherein "said *trench structure and said substrate* receive a control voltage whereby an electric field is produce to control a current *flowing in said diffusion region*," as recited in claims 20 and in similar language in claim 26.

THE REJECTIONS OF CLAIMS 20-27 ARE FLAWED IN THAT IT IMPROPERLY APPLIES THE CONCEPT OF INHERENCY IN AN ATTEMPTS TO CURE THE DEFICIENCIES OF NAKAGAWA et al. REGARDING SUBJECT MATTER WHICH CANNOT BE FOUND THEREIN

In an attempt to overcome the deficiencies of Nakagawa et al. and Yamaguchi, both the Final Rejection and the Examiner's Answer attempts to use an additional reference (i.e., Connor) to show an inherent characteristic of the teaching of Nakagawa et al. In this regard, Section 2131 (III) states:

> [t]o serve as an anticipation when the reference is silent about the asserted inherent characteristic, such gap in the reference may be filled with recourse to extrinsic evidence. Such evidence must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill. *Continental Can Co. USA v. Monsanto Co.,* 948 F.2d 1264, 1268, 20 USPQ2d 1746, 1749 (Fed. Cir. 1991).

However, Section 2112 of the MPEP states:

> [t]he fact that a certain result or characteristic may occur or be present in the prior art is not sufficient to establish the inherency of that result or characteristic. *In re Rijckaert*, 9 F.3d 1531, 1534, 28 USPQ2d 1955, 1957 (Fed. Cir. 1993) (reversed rejection because inherency was based on what would result due to optimization of conditions, not what was necessarily present in the prior art); *In re Oelrich*, 666 F.2d 578, 581-82, 212 USPQ 323, 326 (CCPA 1981).

> "In relying upon the theory of inherency, the examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied prior art." *Ex parte Levy,* 17 USPQ2d 1461, 1464 (Bd. Pat. App. & Inter. 1990) (emphasis added).

The Examiner's Answer attempts to use Conner as an additional reference to prove of the inherent characteristic of an electric field. However, Connor generates an electric field by applying a control voltage between gate **(10, fig. 2)** and substrate **(82, fig. 2)**. In contrast, the claimed invention recites:

> forming electrical connections on said trench structure *and* said substrate which *receive a control voltage whereby an electric field is produced to control a current flowing in said diffusion region* (emphasis added);

For these reasons Appellant requests reversal of the rejection of claim 20-27.

Dated:

Respectfully submitted,

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